Entity sumador8bits is

Port (a:in std\_logic\_vector(7 down to 0);

b:in std\_logic\_vector(7 down to 0);

centrada:in std\_logc;

sumador:out std\_logic (7downto 0);

cout:out std\_logic);

end sumador8bits;

architecture behavioral of sumador8bits is

component sumador is

port (a: in std\_logic;

b:in std\_logic;

centrada:in std\_logic;

sumador:out std\_logic;

cout:out std\_logic);

end component;

signal c:std\_logic\_vector(7downtto1)=(others=>’0’);

c1:sumador port map(a=>(0),b=>(0),centrada=>centrada,sumador=>(0),cout=>(1));

c2:sumador port map(a=>(1),b=>(1),centrada=>(1),sumador=>(1),cout=>(2));

c3:sumador port map(a=>(2),b=>(2),centrada=>(2),sumador=>(2),cout=>(3));

c4:sumador port map(a=>(3),b=>(3),centrada=>(3),sumador=>(3),cout=>(4));

c5:sumador port map(a=>(1),b=>(1),centrada=>(4),sumador=>(4),cout=>(5));

c6:sumador port map(a=>(1),b=>(1),centrada=>(5),sumador=>(5),cout=>(6));

c7:sumador port map(a=>(1),b=>(1),centrada=>(6),sumador=>(6),cout=>(7));

c8:sumador port map(a=>(1),b=>(1),centrada=>(7),sumador=>(7),cout=>(cout));

end behavioral